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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,652	01/18/2002	Ronalf Kramer	1406/36	5317

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,652	KRAMER, RONALF	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1,3-11 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 15-17 objected to because of the following informalities:

In claims 15-17, change "A circuit.." to "The circuit..." Appropriate correction is required.

In claim 16, line 2, change "...transistor..." to "...transistors..."

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, and 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horita et al. (U. S. PAT. 5,469,081).

In claim 1, Horita et al. teaches all claimed features in Fig. 2, a circuit for generating a single asynchronous signal pulse at an output (OP1) of an integrated circuit (11, 12), the circuit comprising: (a) an integrated circuit comprising a push-pull driving circuit (12) having a first and second transistor (MP1, MP2) including control terminals (gate terminals) being independently controlled by different control pulses (output pulse from IN1 and output pulse from IN3) between a first and second supply potential (Vd and ground), and a centre tap (OP1) connected with an output terminal of the integrated circuit; and (b) a single resistor (R) being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein

the type of the resistor determines, by application of a first control pulse (when LG is logic 0, thus logic 0 is at the terminal gate of MP2) on the control terminal of the second transistor and then a second control pulse (logic 1 is at the gate terminal of MP1) on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal, wherein a waiting time (due to the delay of any one inverter) is provided between the first control pulse (logic 0) and the second control pulse (logic 1); with the exception of teaching wherein the two pulses do not overlap. However, it is obvious in the art to apply two pulses that do not overlap, as a matter of adjusting a pulse generator to provide desired output pulses that do not overlap.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to drive the circuit of Horita et al. with two pulses that do not overlap, in order to obtain desirable result as a matter of adjusting the pulse generator that provides the input pulses to the circuit.

In claim 3, Horita et al. further teaches wherein one of the two control pulses (logic 1 at the terminal of MP1) is generated from the other of the two control pulses by an inverter delay device (IN1).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to drive the circuit of Horita et al. with two pulses that do not overlap, in order to obtain desirable result as a matter of adjusting the pulse generator that provides the input pulses to the circuit.

In claims 6-8, Horita et al. teaches all claimed features in Fig. 2, a circuit for generating a negative signal pulse (intended use, no patentable weight given) in response to receiving a sequence of a positive and negative control pulse (logic 1 and logic 0), the circuit comprising: (a) a first transistor (MP1) including a control terminal (gate) and a load path connected between an output terminal (OP1) and a first supply potential (Vd) for receiving a negative control pulse (logic 0) at the control terminal; (b) a second transistor (MP2) including a control terminal (gate) and a load path connected between the output terminal (OP1) and a second supply potential (ground) having a potential less than the first supply potential for receiving a positive control pulse (logic 1) at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and (c) a pull-up resistor (R) connected between the first supply potential and the output terminal for generating a negative signal pulse (intended use) at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses; wherein a waiting time (delay) is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap (due to the delay of any one inverter); and an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to drive the circuit of Horita et al. with two pulses that do not overlap, in order to obtain desirable result as a matter of adjusting the pulse generator that provides the input pulses to the circuit.

Claims 9-11 are essentially the same scope of claims 6-8. Therefore, they are rejected in similarly.

4. Claims 4-5 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horita et al. in view of Taguchi (U. S. PAT. 6,160,417).

In claim 4, Horita et al. teaches all claimed features in Fig. 2 as explained above; with the exception wherein the first transistor is a P-channel MOS transistor and the second transistor is an N-channel MOS transistor. However, Taguchi teaches in Fig. 3 wherein the first transistor (13) is a P-channel MOS transistor and the second transistor (14) is an N-channel MOS transistor, the control connection (the gate electrode) of the first transistor (13) being inverted (PMOS transistor inherently having inverting gate electrode).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to form a push-pull circuit by selecting two different types of transistors instead of using same types of transistors as shown in Fig. 2, circuit 12, of Horita et al., as a matter of design choice based on system involved.

In claim 5, Taguchi further teaches in Fig. 3, the circuit as claimed in claim 4, wherein the first transistor (13) and the second transistor (14) form a CMOS inverter (12) with independent control gate connections (separate gate electrodes).

In claim 15, Taguchi further teaches in Fig. 3, the circuit of claim 1, wherein the first and the second transistors (13, 14) include a source and drain, the drain of the first transistor being connected to the drain of second transistor (as shown in Fig. 3 of Taguchi), the source of the first transistor being connected to the first power potential

(VCC), and the source of the second transistor being connected to the second supply potential (ground).

In claim 16, Taguchi further teaches in Fig. 3, the circuit of claim 6, wherein the first and the second transistors (13, 14) include a source and drain, the drain of the first and second transistors being connected to the output terminal (6), the source of the first transistor being connected to the first supply potential (VCC), and the source of the second transistor being connected to the second supply potential (ground).

In claim 17, Taguchi further teaches in Fig. 3, the circuit of claim 9, wherein the first and the second transistors (13, 14) include a source and drain, the drain of the first and second transistors being connected to the output terminal (6), the source of the first transistor being connected to the first supply potential (VCC), and the source of the second transistor being connected to the second supply potential (ground).

Claims 11-14 are not entered.

typo 12-14

Response to Arguments

2. Applicant's arguments with respect to claims 1 and 9 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1, 3, and 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horita et al., and claims 4-5 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horita et al. in view of Taguchi, as explained above.

The examiner believes the cited references teach all applicant's recited features. The examiner would also like to point out that applicant's figures are very much similar

to the figures in the cited references; therefore, the examiner respectfully believes the circuits in cited reference operate in the same manner as applicant's invented circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

Vibol Tan 

Patent Examiner, AU 2819